



Docket No.: 210067US2

COMMISSIONER FOR PATENTS  
ALEXANDRIA, VIRGINIA 22313



RE: Application Serial No.: 09/883,959  
Applicants: Hidemasa ZAMA, et al.  
Filing Date: June 20, 2001  
For: SEMICONDUCTOR INTEGRATED CIRCUIT,  
LOGIC OPERATION CIRCUIT, AND FLIP FLOP  
Group Art Unit: 2819  
Examiner: TAN, VIBOL

SIR:

Attached hereto for filing are the following papers:

**LETTER SUBMITTING REPLACEMENT DRAWINGS; AND 2 SHEETS OF DRAWINGS.**

Our check in the amount of \$0.00 is attached covering any required fees. In the event any variance exists between the amount enclosed and the Patent Office charges for filing the above-noted documents, including any fees required under 37 C.F.R. 1.136 for any necessary Extension of Time to make the filing of the attached documents timely, please charge or credit the difference to our Deposit Account No. 15-0030. Further, if these papers are not considered timely filed, then a petition is hereby made under 37 C.F.R. 1.136 for the necessary extension of time. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,  
MAIER & NEUSTADT, P.C.

Eckhard H. Kuesters

Registration No. 28,870

Customer Number

**22850**

(703) 413-3000 (phone)

(703) 413-2220 (fax)

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W. Todd Baker

Registration No. 45,265

Docket No.: 210067US2



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

IN RE APPLICATION: Hidemasa ZAMA, et al.

SERIAL NO.: 09/883,959

GAU: 2819

FILED: June 20, 2001

EXAMINER: TAN, VIBOL

FOR: SEMICONDUCTOR INTEGRATED CIRCUIT, LOGIC OPERATION CIRCUIT, AND FLIP FLOP

**LETTER SUBMITTING REPLACEMENT DRAWING SHEET(S)**

COMMISSIONER FOR PATENTS  
Alexandria, VA 22313

SIR:

Responsive to the below indicated communication, the following drawing sheets are submitted herewith:

☒ 2 Replacement Drawing Sheets

☐ \_\_\_\_\_ New Drawing Sheets

☐ Official Action dated \_\_\_\_\_

☐ Notice of Allowance/Issue Fee dated \_\_\_\_\_

☐ Other dated \_\_\_\_\_

The changes and/or modifications made include the following:

Figures 2, 9 and 10 were labeled --Prior Art--.

Respectfully submitted,

Eckhard H. Kuesters

Registration No. 28,870

Customer Number

**22850**

Tel. (703) 413-3000

Fax. (703) 413-2220

(OSMMN 05/2003)

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W. Todd Baker

Registration No. 45,265